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10CS74

Seventh Semester B.E. Degree Examination, June/July 2016
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Define Instruction Set Architecture (ISA). Explain seven dimensions of an ISA. **(10 Marks)**

b. Assume a disk subsystem with the following components and MTTF :
- 10 disks each rated at 1,000,000 hr MTTF
- 1 SCSI controller, 500,000 – hour MTTF
- 1 Power supply, 200,000 – hour MTTF
- 1 Fan, 200, 000 – hour MTTF.
- 1 SCSI cable, 1,000,000 – hour MTTF.

Using the simplifying assumptions that the lifetimes are exponentially distributed and that failures are independent, compute the MTTF of the system as a whole. **(05 Marks)**

c. List and explain four important technologies, which change at a dramatic pace and are critical to modern implementation. **(05 Marks)**

2 a. With a neat diagram, explain the classic five stage pipeline for a RISC processor. **(10 Marks)**

b. List three major hurdles of pipelining. Explain the concept of minimizing data hazards stalls by forwarding using the example below :

```
DADD    R1, R2, R3
DSUB    R4, R1, R5
AND     R6, R1, R7
OR      R8, R1, R9
XOR     R10, R1, R11.
```

(10 Marks)

3 a. Show how the below loop would look on MIPS 5 – stage pipeline, under the following situations. Also find the number of cycles per iteration for each case. Latency of LOAD is 2, ADD.D is 3, store is 1, DADDUI is 2 and Branches is 1. **(12 Marks)**

```
Loop :  L.D     F0, 0(R1)
        ADD.D   F4, F0, F2
        SD      F4, 0(R1)
        DADDUI  R1, R1, # -8
        BNE     R1, R2, Loop
```

i) Without scheduling, without unrolling ii) With scheduling, without unrolling.
iii) With loop unrolling, without scheduling iv) With loop unrolling, with scheduling.

b. What is the drawback of 1 – bit dynamic branch prediction method? Clearly state how it is overcome in 2 – bit prediction. Give the state transition diagram of 2 – bit predictor. **(08 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, with multiple issues using the following example. We have a VLIW that could issue two memory references, two FP operations and one integer or branch every clock cycle. Use the unrolled version of the code given in question 3a. How many clock cycles per result does it require? **(10 Marks)**

b. What is Branch Target Buffer? With a neat diagram, explain the steps when using BTB. **(10 Marks)**

PART – B

5 a. With the help of neat diagram, explain the basic structure of centralized shared memory and distributed memory multiprocessor. **(10 Marks)**

b. Explain directory based cache coherence for a distributed memory multiprocessor system along with the state transition diagram. **(10 Marks)**

6 a. List the basic cache optimization techniques. Explain any four. **(10 Marks)**

b. Assume we have a computer where the CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? **(10 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain multibanked caches to increase cache bandwidth. **(10 Marks)**

b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. **(10 Marks)**

8 a. Explain the architecture of IA64 intel processor and also the prediction and speculation support provided. **(10 Marks)**

b. Explain in detail, the hardware support for preserving exception behavoiur during speculation. **(10 Marks)**

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